REMARKS

The following remarks are responsive to the April 20, 2005 Office Action. Claims 3 and 4 remain as previously presented. Please reconsider the claims in view of the following remarks.

Response to Rejection of Claims 3 and 4 Under 35 U.S.C. § 102(b)

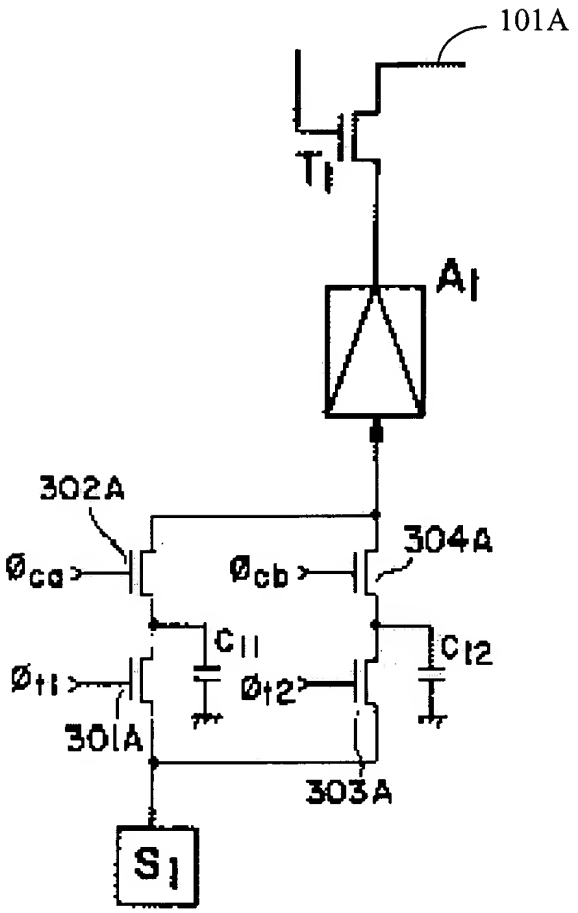
In the April 20, 2005 Office Action, the Examiner rejects Claims 3 and 4 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,311,320 issued to Hashimoto ("Hashimoto"). The Examiner states that Hashimoto discloses all the limitations of Claims 3 and 4.

Claim 3 recites (emphasis added):

> 3. An image sensor comprising an array of columns and rows of pixels (X_{ij}), **all the pixels of one column of the array being connected to at least one common pixel output line** (1_j) having at least one memory element (M_j) and at least one column amplifying element (A_j), all said column amplifying elements (A_j) being connected to a common output amplifier (D), **each common pixel output line** (1_j) **being divided through switches** ($S4_j$ and $S5_j$) **into at least two parallel circuits before the respective column amplifying element** (A_j), at least one of these parallel circuits having said memory element (M_j), **the two parallel circuits being connected through a switch** ($S6_j$) **with the same input of said column amplifying element** (A_j), said column amplifying elements (A_j) and the common output amplifier (D) being connected by a single bus, wherein there is a further switch (X_j) between said column amplifying element (A_j) and said bus, and wherein the image sensor is a CMOS or MOS device.

Contrary to what the Examiner indicates, Hashimoto does not disclose or suggest an image sensor having "all the pixels of one column of the array being connected to at least one common pixel output line," "each common pixel output line ... being divided through switches ... into at least two parallel circuits before the respective column amplifying element," and "the two parallel circuits being connected through a switch ... with the same input of said column amplifying element," as recited by Claim 3.

The Examiner combines various elements from Figure 16A with various elements from Figure 18 of Hashimoto to support the rejection of Claim 3. However, if Figure 18 of Hashimoto is combined with Figure 16A of Hashimoto, then the following schematic circuit diagram would be obtained:



This schematic circuit diagram is applicable to each photosensor circuit, and all such circuits are then connected up to the common output line 101A, as shown in Figure 16A of Hashimoto.

This schematic circuit diagram is supported by column 20, lines 41-43 of Hashimoto, which discloses that "[t]he switches SW1 to SWn respectively receive sensor signals S1 to Sn from photosensors S1 to Sn arranged in a line or a matrix form." In particular, this passage of Hashimoto discloses that even if a matrix is used, the number of switches equals the number of photosensors, i.e., there are **no common column lines with which a switch would be shared among several photosensors**. In the implementation illustrated by Figure 16A of Hashimoto, the photosensors are arranged in line form. However, if they would be arranged in matrix form, then Hashimoto teaches having one switch SWj for every photosensor Sj, i.e., having as many switches as there are photosensors. The combination of the "switch Sj" with the "amplifier Aj" cited by the Examiner corresponds to a pixel output line having at least one memory element and at least one amplifying element, with each pixel output line being divided through switches into at least two parallel circuits before the respective column amplifying elements, as shown

hereinabove in the combination of Figures 16A and 18 of Hashimoto. However, the combination does not have "all the pixels of one column of the array being connected to at least one **common** pixel output line," as recited by Claim 3 (emphasis added).

Hashimoto does discuss the implementation of common column lines in other embodiments of their invention. Hashimoto discloses an embodiment having a matrix of pixels with all the pixels on a column being connected to a common pixel output line (vertical lines VL1 and VL2 shown in Figure 28). In this embodiment, no column amplifying elements are present on the common pixel output lines, and there is no common output amplifier to which the common pixel output lines are connected via a switch. The vertical lines VL1 and VL2 are connected to readout circuits R1 and R2, respectively, as shown in Figure 28. These readout circuits are detailed in Figure 29 of Hashimoto, from which it can be seen that the vertical line VLi is divided through switches Qt1, ..., Qt4 into at least two parallel circuits (4 parallel circuits shown in Figure 29). However, these parallel circuits are not "connected through a switch ... with the same input of said column amplifying element," as recited by Claim 3.

Hashimoto is a very detailed document which provides a detailed discussion of various possibile structures for line and matrix configurations of the photosensitive elements. For lines or small matrices of pixels, Hashimoto teaches a structure having a pixel output line for each pixel, each pixel output line having at least one memory element and at least one amplifying element and being divided through switches into at least two parallel circuits before the column amplifying element. Thus, two parallel circuits are implemented for **every** photosensitive element. However, Hashimoto does not disclose that such a structure has a common column line. For larger matrices, Hashimoto teaches an alternative structure with a common column line per column which connects all the pixels of a column, but in which the complete circuit is changed so as to read out a signal of two or more horizontal lines (see, e.g., col. 29 lines 6-10 of Hashimoto) with a plurality of output lines and a plurality of output amplifiers. Thus, each column line is divided through switches into a plurality of parallel circuits having a plurality of output amplifiers. However, Hashimoto does not disclose that such an alternative structure has the parallel circuits connected through a switch with the same input as the column amplifying element.

Applicants submit that the complete teachings of Hashimoto do not teach the structure recited by Claim 3. Even combined with his general knowledge, a person skilled in the art would

not, based on the teachings of Hashimoto, come to the structure recited by Claim 3. Therefore, Applicants submit that Claim 3 is patentable over Hashimoto. Claim 4 depends from Claim 3, so Claim 4 includes all the limitations of Claim 3 as well as other limitations of particular utility. For at least the reasons discussed above, Applicants submit that Claim 4 is also patentable over Hashimoto. Applicants respectfully request that the Examiner withdraw the rejection of Claims 3 and 4 and pass these claims to allowance.

Summary

For the foregoing reasons, Applicants submit that Claims 3 and 4 are in condition for allowance, and Applicants respectfully request such action.

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

Dated: 8/22/05 By: _____

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